ADM-PCIE-9V3
User Manual

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1 Introduction

The ADM-PCIE-9V3 is a high-performance reconfigurable computing card intended for Data Center applications, featuring a Xilinx Virtex UltraScale Plus FPGA.

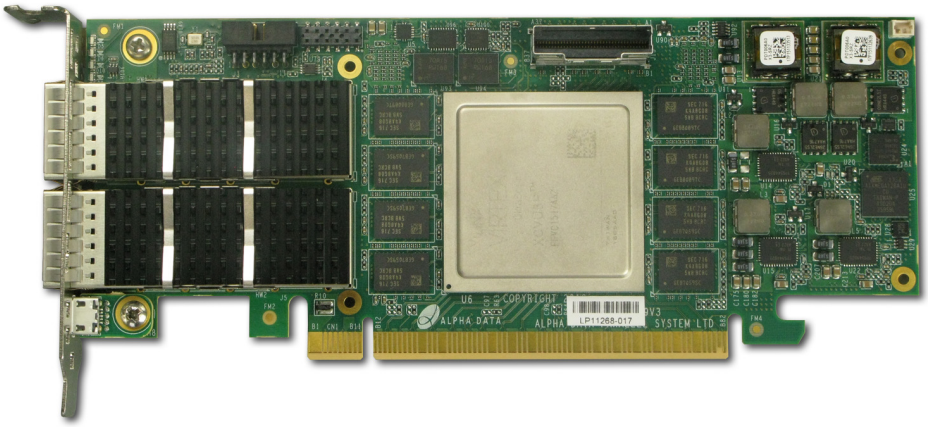

Figure 1 : ADM-PCIE-9V3 Product Photo

1.1 Key Features

Key Features

- PCIe Gen1/2/3 x1/2/4/8/16 capable
- Half-length, low-profile x16 PCIe form factor
- Two banks of DDR4 SDRAM 72 bit wide memory (ECC), 16GB (8GB per bank) default rated at 2400MT/s, 32GB option rated at 1866MT/s.
- Two QSFP28/zQSFP+ sites capable of data rates up to 28 Gbps per channel (112 Gbps per cage)
- One 8 lane Ultraport SlimSAS connector that is compliant with OpenCAPI
- Optional timing input
- Front panel and rear edge JTAG access via USB port
- FPGA configurable over USB/JTAG and SPI configuration flash
- XCVU3P-2FFVC1517E FPGA
- Voltage, current, and temperature monitoring

1.2 Order Code

ADM-PCIE-9V3

See http://www.alpha-data.com/pdfs/adm-pcie-9v3.pdf for complete ordering options.

2 PCB Information

2.1 Physical Specifications

The ADM-PCIE-9V3 complies with PCI Express CEM revision 3.0.

Description	Measure
PCB Dy	64.4 mm
PCB Dx	167.65 mm
PCB Dz	1.6 mm

Table 1 : Mechanical Dimensions (PCB only)

Description	Measure
Total Dy	68.9 mm
Total Dx (Inc. QSFP Cages)	174 mm
Total Dz	17.45 mm
Weight	230 grams

Table 2 : Mechanical Dimensions

2.2 Chassis Requirements

2.2.1 PCI Express

The ADM-PCIE-9V3 is capable of PCIe Gen 1/2/3 with 1/2/4/8/16 lanes, using the Xilinx Integrated Block for PCI Express.

2.2.2 Mechanical Requirements

A 16-lane physical PCIe slot is required for mechanical compatibility.

Each ADM-PCIE-9V3 is shipped with a full height PCIe card bracket installed by default. A half-height bracket is shipped along with the product and can be easily changed out with a Philips screw driver. If the application requires a low-profile bracket and the order quantity is high, contact sales@alpha-data.com to get the correct bracket fitted before shipping.

2.2.3 Power Requirements

The PCIe Specification permits a standard low-profile, half-length PCIe card to dissipate up to 25 W of power, drawn from the PCIe slot. The ADM-PCIE-9V3 may consume more than 25 W of power for larger user FPGA designs. Power estimation requires the use of the Xilinx XPE spreadsheet and/or a power estimator tool available from Alpha Data. Please contact **support@alpha-data.com** to obtain this tool.

The power available to the rails calculated using XPE are as follows:

Voltage	Source Name	Current Capability
0.85	VCC_INT + VCCINT_IO + VCC_BRAM	36A
1.8	VCCAUX + VCCAUX_IO + VCC_BRAM + VCCO_1.8V	6A
3.3	VCCO_3.3V	6A
1.2	VCCO_1.2V	9A
1.8	MGTVCCAUX	1A
0.9	MGTAVCC	9A
1.2	MGTAVTT	15A

Table 3 : Available Power By Rail

2.3 Thermal Performance

If the FPGA core temperature exceeds 100 degrees Celsius, the FPGA design will be cleared to prevent that card from over-heating.

The ADM-PCIE-9V3 comes with a heat sink to reduce the heat of the FPGA which is typically the hottest point on the card. The FPGA die temperature must remain under 100 degrees Celsius. To calculate the FPGA die temperature, take your application power and multiply by Theta JA from the table below, and add to your system internal ambient temperature. If you are using the fan provided with the board, you will find theta JA is approximately 1.4 degC/W for the board in still air.

The power dissipation can be estimated by using the Alpha Data power estimator in conjunction with the Xilinx Power Estimator (XPE) downloadable at http://www.xilinx.com/products/technology/power/xpe.html. Download the UltraScale tool and set the Device to Virtex UltraScale+, VU3P, FFVC1516, -2, Industrial. Set the ambient temperature to your system ambient and select User Override for the Effective theta JA and enter the figure associated with your system LFM in the blank field. Proceed to enter all applicable design elements and utilization in the following spreadsheet tabs. Next aquire the 9V3 power estimator from Alpha Data by contacting support@alpha-data.com. You will then plug in the FPGA power figures along with DDR4 and QSFP usage to get an estimate.

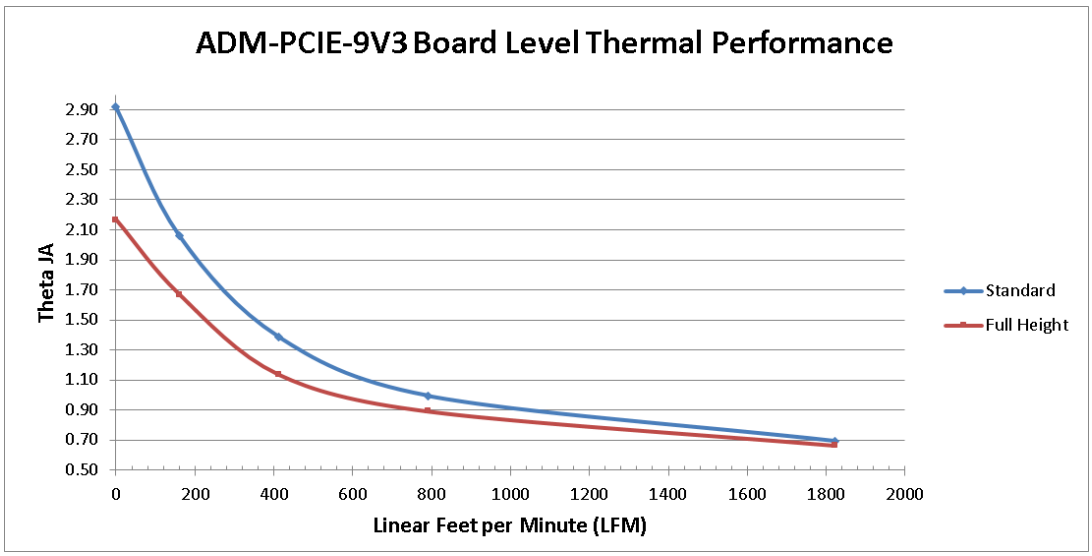

Figure 2 : Thermal Performance

2.4 Optional Blower

Because it is possible for generic PC chassis to not provide sufficient airflow to cool the FPGA, the ADM-PCIE-9V3 is shipped with an uninstalled blower. The blower is optional and can be easily installed with a Philips screw driver at the discretion of the user. Ensure the opening is facing the heatsink fins. The blower hangs off the back of the PCB outside of the PCIe card envelope. After screwing the blower into the heatsink, plug in the small power connector into the connector in the corner of the board. It is possible to alternatively ship a fan that fits in the adjacent PCIe card slot if required for mechanical fit, contact sales@alpha-data.com for details.

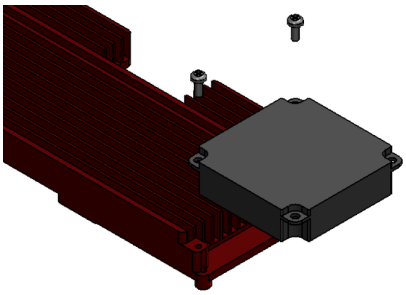

Figure 3 : Optional Blower

2.5 Full Height Heat Sink

For customers with full height chassis that would like better thermal performance, and to baffle the empty space above the card, Alpha Data sells a full height heat sink variant. The thermal performance boost is documented in the Thermal Performance image above. Contact sales@alpha-data.com for more details.

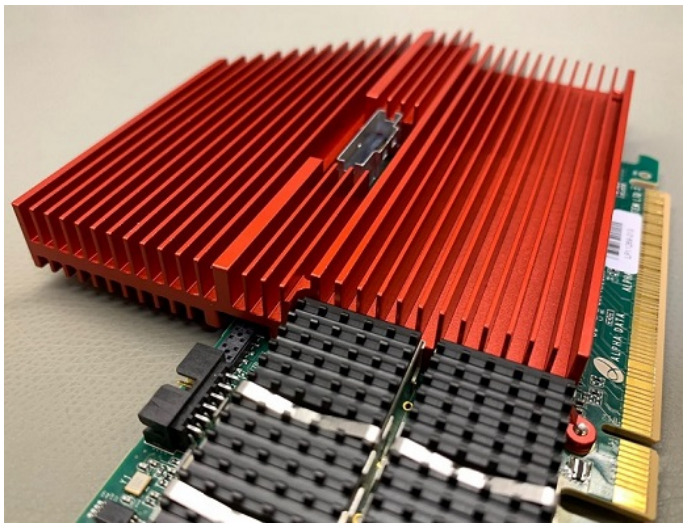

Figure 4 : Full Height Heat Sink

3 Functional Description

3.1 Overview

The ADM-PCIE-9V3 is a versatile reconfigurable computing platform with a Virtex UltraScale VU3P FPGA, a Gen3x16 PCIe interface, two banks of DDR4 both 72 bits wide (for 64 bits with 8 bits ECC), two QSFP28 cages capable of 8x 28G or 2x 112G Serial IO of any Xilinx supported standard (Ethernet, SRIO, Infiniband, etc.), one OpenCAPI compatible Ultraport SlimSAS connector also capable of 28G/channel, an input for a timing synchronization input, a 12 pin header for general purpose use (clocking, control pins, debug, etc.), and a robust system monitor.

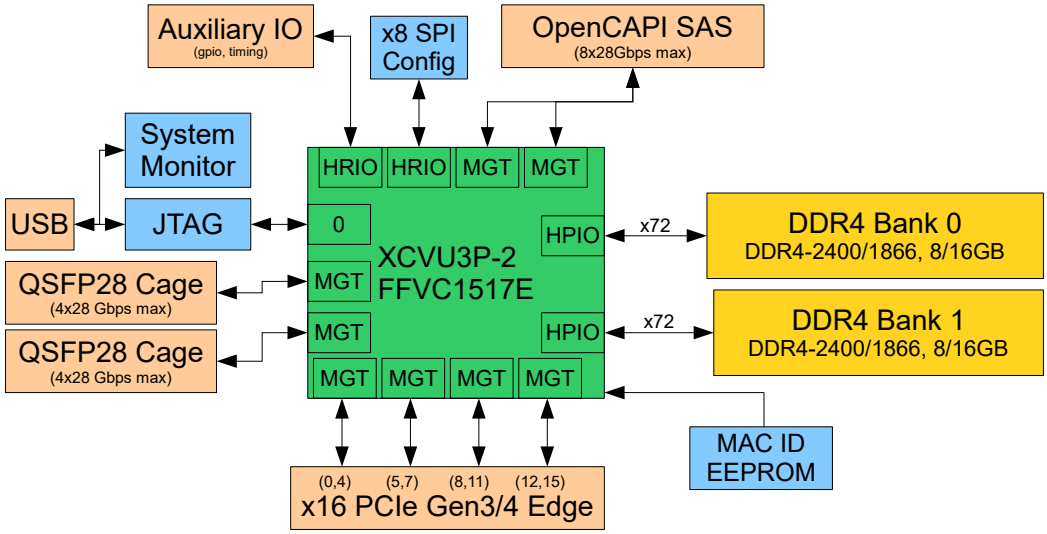

Figure 5 : ADM-PCIE-9V3 Block Diagram

3.1.1 Switches

The ADM-PCIE-9V3 has a quad DIP switch SW1, located on the rear side of the board. The function of each switch in SW1 is detailed below:

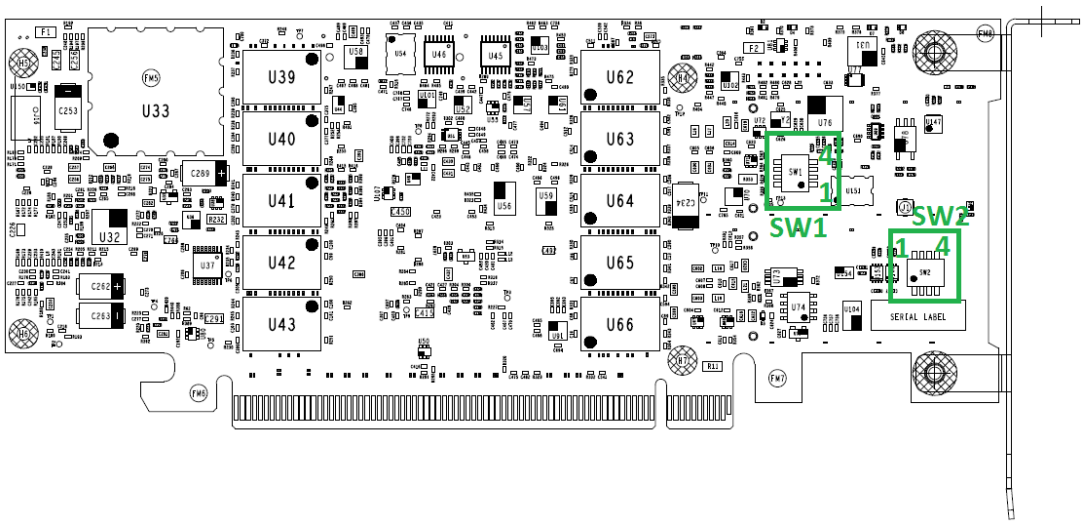

Figure 6 : Switches

Switch	Factory Default	Function	OFF State	ON State
SW1-1	OFF	User Switch 0	Pin AV27 = '1'	Pin AV27 = '0'
SW1-2	OFF	User Switch 1	Pin AW27 = '1'	Pin AW27 = '0'
SW1-3	OFF	Service Mode	Regular Operation	Firmware update service mode
SW1-4	OFF	JTAG Source	JTAG to FPGA from USB	JTAG to FPGA from debug header
SW2-1	ON	HOST_I2-C_EN	Sysmon over PCIe I2C	Sysmon isolated
SW2-2	ON	CAPI_VP-D_EN	OpenCAPI VPD available	OpenCAPI VPD isolated
SW2-3	ON	CAPI_VP-D_WP	CAPI VPD is write protected	CAPI VPD is writable
SW2-4	ON	Reserved	Reserved	Reserved

Table 4 : Switch Functions

Use IO Standard "LVCMOS18" when constraining the user switch pin.

3.1.2 LEDs

There are 8 LEDs on the ADM-PCIE-9V3, 5 of which are general purpose and whose meaning can be defined by the user. The other 3 have fixed functions described below:

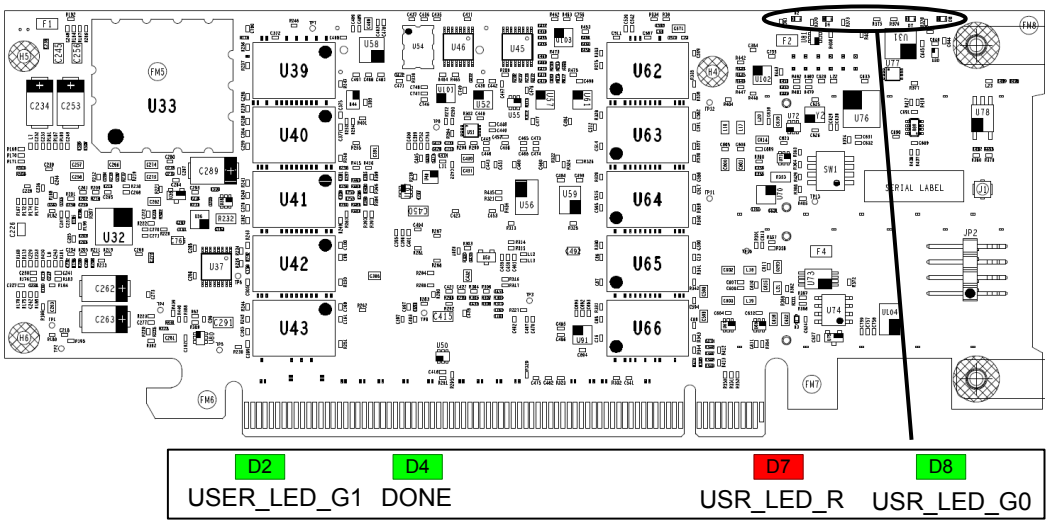

Figure 7 : Backside LEDs

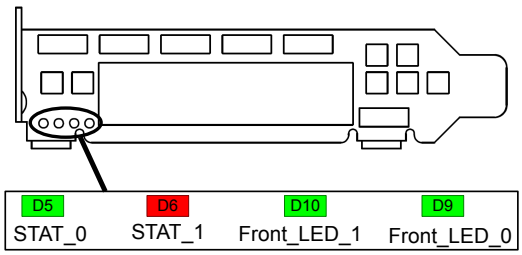

Figure 8 : Front Panel LEDs

Comp. Ref.	Function	ON State	OFF State
D4	DONE	FPGA is configured	FPGA is not configured
D8	USER_LED_G0	User defined '0' pin AT27	User defined '1' pin AT27
D2	USER_LED_G1	User defined '0' pin AU27	User defined '1' pin AU27
D7	USER_LED_R	User defined '0' pin AU23	User defined '1' pin AU23
D5	Status 0	See Status LED Definitions	
D6	Status 1	See Status LED Definitions	
D9	Front_LED_0	User defined '1' pin AH24	User defined '0' pin AH24
D10	Front_LED_1	User defined '1' pin AJ23	User defined '0' pin AJ23

Table 5 : LED Details

Use IO Standard "LVCMOS18" when driving the user LED pins.

3.2 Clocking

The ADM-PCIE-9V3 provides reference clocks for the DDR4 SDRAM banks and the I/O interfaces available to the user. After a clock is programmed to a certain frequency, that frequency will become the default on power-up. Any clock out of an Si5338 Clock Synthesizer is re-configurable from either the front panel USB USB Interface or the Alpha Data bridge IP available in the board support package (sold separately). This allows the user to configure almost any arbitrary clock frequencies during application run time. Maximum clock frequency is 312.5MHz.

Note: use "set_property BITSTREAM.CONFIG.UNUSEDPIN {Pullnone} [current_design]" to ensure the user design does not interfere with the I2C interface to the reprogramable clock generator.

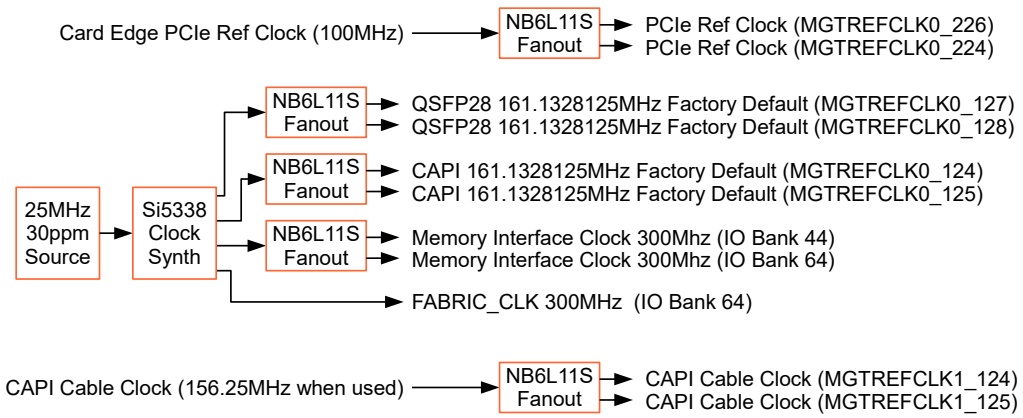

Figure 9 : Clock Topology

3.2.1 PCIe Reference Clocks

The 16 MGT lanes connected to the PCIe card edge use MGT quads 224 through 227 and use the system 100 MHz clock (PCIE_REFCLK).

Signal	Target FPGA Input	I/O Standard	"P" pin	"N" pin
PCIE_REFCLK1	MGTREFCLK0_226	HCSL	AA7	AA6
PCIE_REFCLK2	MGTREFCLK0_224	HCSL	AJ7	AJ6

Table 6 : PCIe Reference Clocks

3.2.2 Fabric Clock

The design offers a fabric clock called FABRIC_CLK which is permanently fixed at 300 MHz. This clock is intended to be used for IDELAY elements in FPGA designs. The fabric clock is connected to a Global Clock (GC) pin.

Signal	Target FPGA Input	I/O Standard	"P" pin	"N" pin
FABRIC_CLK	IO_L12P_T1U_GC_64	LVDS	AP26	AP27

Table 7 : Fabric Clock

DIFF_TERM_ADV = TERM_100 is required for LVDS termination

3.2.3 Programming Clock (EMCCLK)

An 100MHz clock is fed into the EMCCLK pin to drive the SPI flash device during configuration of the FPGA. Note that this is not a global clock capable IO pin.

Signal	Target FPGA Input	I/O Standard	pin
REFCLK100M	IO_L24P_T3U_N10_EMCCLK_65	LVCMOS18	AJ28

Table 8 : EMCCLK

3.2.4 QSFP28

The QSFP28 cages are located in MGT quads 127 and 128 and use a 161.1328125MHz default reference clock. Note that this clock frequency can be changed to any arbitrary clock frequency up to 312MHz by re-programing the Si5338 reprogrammable clock oscillator via system monitor. This can be done using the Alpha Data API or over USB with the appropriate Alpha Data Software tools.

Signal	Target FPGA Input	I/O Standard	"P" pin	"N" pin
GTY_CLK_0B	MGTREFCLK0_128	LVDS	N33	N34
GTY_CLK_0C	MGTREFCLK0_127	LVDS	U33	U34

Table 9 : QSFP28 Reference Clocks

The QSFP28 cages are also located such that they can be clocked from a Si5328 jitter attenuator clock multiplier. If jitter attenuation is required please see the reference documentation for the Si5328. https://www.silabs.com/Support%20Documents/TechnicalDocs/Si5328.pdf

The Si5328 is configured with a 114.285MHz oscilator on XA and XB

The Si5328 SDA pin connects at FPGA pin L29 (1.8V), SCL is at FPGA pin L30 (1.8V) with external pull-ups included.

The Si5328 can be reached at I2C address 1101000

The Si5328 input clock comes from FPGA pins M29 and M30, and includes 100 Ohm differential termination and 100nF AC coupled termination from the 1.8V FPGA bank suitable for LVDS signal levels.

The Si5328 output clocks are AC coupled with 10nF capacitors and then connected to the FPGA MGTREFCLK pins shown in the table below. LVDS signal standard is recommended on these nets as well.

Signal	Target FPGA Input	I/O Standard	"P" pin	"N" pin
SI5328_REFCLK_OUT0	MGTREFCLK1_128	LVDS	L33	L34
SI5328_REFCLK_OUT1	MGTREFCLK1_127	LVDS	R33	R34

Table 10 : QSFP28 Jitter Attenuated Reference Clocks

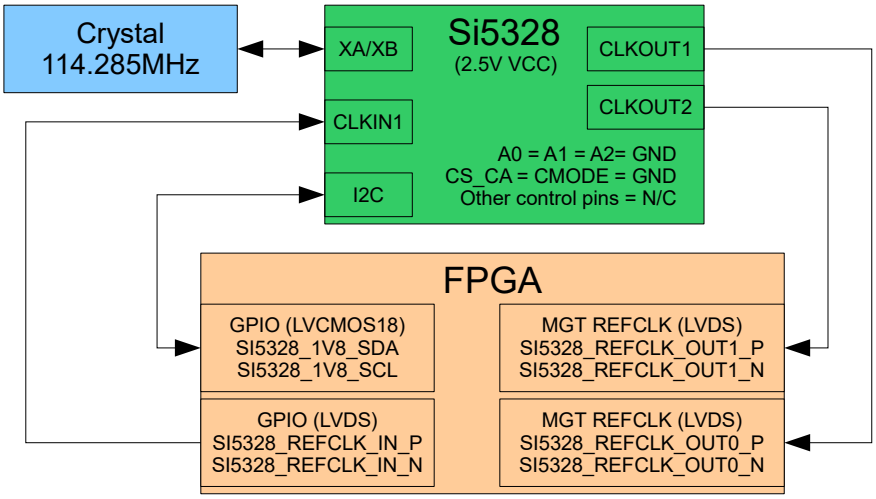

Figure 10 : Si5328 Block Diagram

3.2.5 Ultraport SlimSAS

The Ultraport SlimSAS connector is located in MGT quads 124 and 125 and use a 161.1328125MHz default reference clock. Note that this clock frequency can be changed to any arbitrary clock frequency up to 312MHz by re-programing the Si5338 reprogrammable clock oscillator via system monitor. This can be done using the Alpha Data API or over USB with the appropriate Alpha Data Software tools.

Signal	Target FPGA Input	I/O Standard	"P" pin	"N" pin
GTY_CLK_1B	MGTREFCLK0_125	HCSL	AE33	AE34
GTY_CLK_1C	MGTREFCLK0_124	HCSL	AJ33	AJ34
CAPI_CLK_C	MGTREFCLK1_125	HCSL	AC33	AC34
CAPI_CLK_D	MGTREFCLK1_124	HCSL	AG33	AG34

Table 11 : SlimSAS Reference Clocks (OpenCAPI)

3.2.6 DDR4 SDRAM Reference Clocks

The two banks of DDR4 SDRAM memory each require a separate reference clock, as per Xilinx UltraScale MIG design guidelines. The reference clocks for these interfaces are detailed below:

Both clocks are 300MHz by default.

Signal	Target FPGA Input	I/O Standard	"P" pin	"N" pin
MEM_CLK_0	IO_L13_T2L_GC_44	LVDS	G31	G32
MEM_CLK_1	IO_L11_T2L_GC_64	LVDS	AN25	AN26

Table 12 : Memory Reference Clocks

DIFF_TERM_ADV = TERM_100 is required for LVDS termination

3.3 PCI Express

The ADM-PCIE-9V3 is capable of PCIe Gen 1/2/3 with 1/2/4/8/16 lanes. The FPGA drives these lanes directly using the Integrated PCI Express block from Xilinx. Negotiation of PCIe link speed and number of lanes used is generally automatic and does not require user intervention.

PCI Express reset (PERST#) connected to the FPGA at two locations. See Complete Pinout Table signals PERST_1V8_0 and PERST_1V8_1.

The other pin assignments for the high speed lanes are provided in the pinout attached to the Complete Pinout Table

The PCI Express specification requires that all add-in cards be ready for enumeration within 120ms after power is valid (100ms after power is valid + 20ms after PERST is released). The ADM-PCIE-9V3 does meet this requirement when configured from a tandem bitstream with the proper SPI constraints detailed in the section: Configuration From Flash Memory. For more details on tandem configuration, see Xilinx xapp 1179.

Note:
Different motherboards/backplanes will benefit from different RX equalization schemes within the PCIe IP core provided by Xilinx. Alpha Data recommends using the following setting if a user experiences link errors or training issues with their system: within the IP core generator, change the mode to "Advanced" and open the "GT Settings" tab, change the "form factor driven insertion loss adjustment" from "Add-in Card" to "Chip-to-Chip" (See Xilinx PG239 for more details).

3.4 DDR4 SDRAM

Two banks of DDR4 SDRAM memory are soldered down to the board. While the factory default is 8GB/per bank, 16GB/bank is also supported through a built variant. Please see Order Code for all order options. The memory interface is 72-bit wide data (64 data + 8 ECC). Maximum signaling rate is 2400 MT/s for 16GB total and 2133MT/s with 32GB total.

Memory solutions are available from the Xilinx Memory Interface Generator (MIG) tool. An example memory exerciser project is included in the ADM-PCIE-9V3 SDK. All constraint information is included in Complete Pinout Table. Alpha Data has also provided a custom csv timing file for use with Xilinx MIG. This can be downloaded from the ADM-PCIE-9V3 product page.

8Gb components used (standard) are Samsung K4A8G085WB-BCRC

16Gb components used (build variant) are Micron MT40A2G8PM-093E

When using the timing files provided on the alpha data product page custom_parts_2400.csv, always use the samsung timing files, as they are more relaxed than the micron variants.

3.5 QSFP28

Two QSFP28 cages are available at the front panel. Both cages are capable of housing either active optical or passive copper QSFP28 or QSFP compatible components. The communication interface can run at up to 28Gbps per channel. There are eight channels between the two QSFP28 cages (total maximum bandwidth of 224Gbps). These cages are ideally suited for 8x 25G or 2x 100G Ethernet or any other protocol supported by the Xilinx GTY Transceivers. Please see Xilinx User Guide UG578 for more details on the capabilities of the transceivers.

Both QSFP28 cages have control signals connected to the FPGA. Their connectivity is detailed in the Complete Pinout Table at the end of this document. The notation used in the pin assignments is QSFP0 and QSFP1 with locations clarified in the diagram below.

Use the QSFP*_SEL_1V8_L in conjunction with the OPTICAL_SCL_1V8 and OPTICAL_SDA_1V8 pins as detailed in Complete Pinout Table to communicate with QSFP28 register space.

Note:
The LP_MODE (Low Power Mode) to each QSFP28 cage is tied to ground.

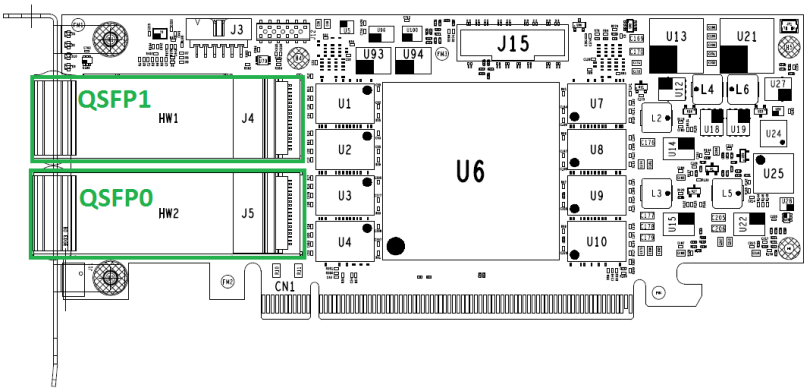

Figure 11 : QSFP Locations

The order options for the ADM-PCIE-9V3 include an option to fit the QSFP28 optical transceivers. The table below shows the part number for the transceivers fitted with each option.

Order Code	Description	Part Number	Manufacturer
Q10	40G (4x10) QSFP Optical Transceiver	FTL410QE2C	Finisar
Q14	56G (4x14) QSFP Optical Transceiver	FTL414QB2C	Finisar
Q25	100G (4x25) QSFP28 Optical Transceiver	FTLC9551REPM	Finisar

Table 13 : QSFP28 Part Numbers

3.6 OpenCAPI Ultraport SlimSAS

An Ultraport SlimSAS receptacles along the top of the board allows for OpenCAPI compliant interfaces running at 200G (8 chanels at 25G). Please contact support@alpha-data.com or your IBM representative for more details on OpenCAPI and its benefits.

The SlimSAS connector can also be used to connect multiple 9V3 cards within a chassis.

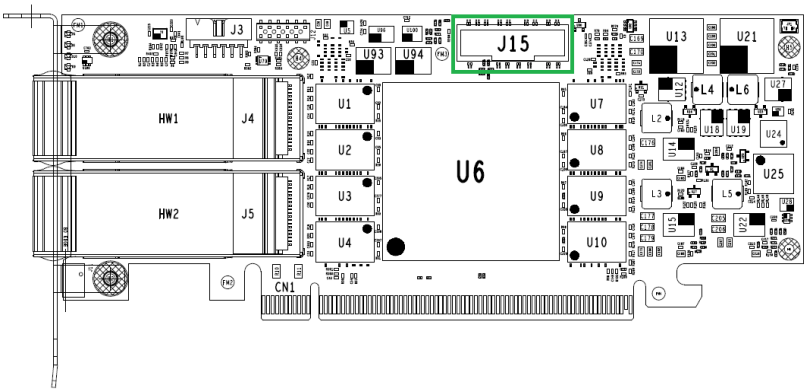

Figure 12 : OpenCAPI Location

3.7 System Monitor

The ADM-PCIE-9V3 has the ability to monitor temperature, voltage, and current of the system to check on the operation of the board. The monitoring is implemented using an Atmel AVR microcontroller.

If the core FPGA temperature exceeds 100 degrees Celsius, the FPGA will be cleared to prevent damage to the card.

Control algorithms within the microcontroller automatically check line voltages and on board temperatures and shares makes the information available to the FPGA over a dedicated serial interface built into the Alpha Data reference design package (sold separately). The information can also be accessed directly from the microcontroller over the USB interface on the front panel or via the IPMI interface available at the PCIe card edge.

Monitors	Index	Purpose/Description
ETC	ETC	Elapsed time counter (seconds)
EC	EC	Event counter (power cycles)
12.0V	ADC00	Board Input Supply
3.3V	ADC01	Board Input Supply
3.3V	ADC02	Board Input Auxilary Power Supply
3.3V	PSU0OK	Internal logic voltage
2.5V	ADC03	Clock and DRAM Voltage Supply
1.8V	PSU0OK	FPGA IO Voltage (VCCO)
1.8V	ADC04	Transceiver Power (AVCC_AUX)
1.2V	ADC05	DDR4 SDRAM and FPGA memory I/O
1.2V	ADC06	Transceiver Power (AVTT)
0.9V	ADC07	Transceiver Power (AVCC)
0.85V	ADC08	FPGA Core Supply (VccINT)
0.6V	ADC09	DDR4 Termination Voltage
12V_I	ADC10	12V input current in amps
3.3V_I	ADC11	3.3V input current in amps
1.8V_MGT_I	ADC12	1.8V MGT supply current in amps
2.5V_DIG_I	ADC13	2.5V supply current in amps
uC_Temp	TMP00	FPGA on-die temperature
Board0_Temp	TMP01	Board temperature near front panel
Board1_Temp	TMP02	Board temperature near back top corner
FPGA_Temp	TMP03	FPGA on-die temperature

Table 14 : Voltage, Current, and Temperature Monitors

3.7.1 System Monitor Status LEDs

LEDs D6 (Red) and D5 (Green) indicate the card health status.

LEDs	*Status*
Green	Running and no alarms
Green + Red	Standby (Powered off)
Flashing Green + Flashing Red (together)	Attention - critical alarm active
Flashing Green + Flashing Red (alternating)	Service Mode
Flashing Green + Red	Attention - alarm active
Red	Missing application firmware or invalid firmware
Flashing Red	FPGA configuration cleared to protect board

Table 15 : Status LED Definitions

3.8 USB Interface

For convenience the FPGA can be configured directly from the USB connection on either the front panel or the rear card edge (rear edge in rev7, sn306 and newer). The ADM-PCIE-9V3 utilizes the Digilent USB-JTAG converter box which is supported by the Xilinx software tool suite. Simply connect a micro-USB AB type cable between the ADM-PCIE-9V3 USB port and a host computer with Vivado installed. Vivado Hardware Manager will automatically recognize the FPGA and allow you to configure the FPGA and the SBPI configuration PROM.

The same USB connector is used to directly access the system monitor system. All voltages, currents, temperatures, and non-volatile clock configuration settings can be accessed using Alpha Data's avr2util software at this interface.

Avr2util for linux and windows (including USB driver) is downloadable at the following links:
https://support.alpha-data.com/pub/firmware/utilities/windows/
https://support.alpha-data.com/pub/firmware/utilities/linux/

Use "avr2util.exe /?" to see all options.

For example "avr2util.exe /usbcom com4 display-sensors" will desiplay all sensor values.

For example "avr2util.exe /usbcom com4 setclknv 0 156250000" will set the QSFP clock to 156.25MHz. setclk index 1 = CAPI, index 2 = Memory, index 3 = Fabric.

Change 'com4' to match the com port number assigned under windows device manager.

3.9 Configuration

There are two main ways of configuring the FPGA on the ADM-PCIE-9V3:

- From Flash memory, at power-on, as described in Section 3.9.1
- Using USB cable connected at either USB port Section 3.9.2

3.9.1 Configuration From Flash Memory

The FPGA can be automatically configured at power-on from two 256 Mbit QSPI flash memory device configured as an x8 SPI device (Micron part numbers MT25QU256ABA8E12-1SIT). These flash devices are typically divided into two regions of 32 MiByte each, where each region is sufficiently large to hold an uncompressed bitstream for a VU3P FPGA.

The ADM-PCIE-9V3 is shipped with a simple PCIe endpoint bitstream containing a basic Alpha Data ADXDMA bitstream. Alpha Data can load in other custom bitstreams during production test, please contact sales@alpha-data.com for more details.

It is possible to use Multiboot with a fallback image on this hardware. The master SPI configuration interface and the Fallback MultiBoot are discussed in detail in Xilinx UG570.

At power-on, the FPGA attempts to configure itself automatically in serial master mode based on the contents of the header in the programing file. Multibook and ICAP can be used to selected between the two configuration regions to be loaded into the FPGA. See Xilinx UG570 MultiBoot for details.

The image loaded can also support tandem PROM or tandem PCIE with field update configuration methods. These options reduce power-on load times to help meet the PCIe reset timing requirements. Tandem with field also enables a host system to reconfigure the user FPGA logic without losing the PCIe link, a useful feature when system resets and power cycles are not an option.

The Alpha Data System Monitor is also capable of reconfiguring the flash memory and reprograming the FPGA. This provides a useful failsafe mechanism to re-program the FPGA even if it drops off the PCIe bus. The system monitor can be accessed over USB at the front panel and rear edge, or over the SMBUS connections on the PCIe edge.

3.9.1.1 Building and Programming Configuration Images

Generate a bitfile with these constraints (see xapp1233):

- set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
- set_property BITSTREAM.CONFIG.EXTMASTERCCLK_EN {DIV-1} [current_design]
- set_property BITSTREAM.CONFIG.SPI_32BIT_ADDR YES [current_design]
- set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 8 [current_design]
- set_property BITSTREAM.CONFIG.SPI_FALL_EDGE YES [current_design]
- set_property BITSTREAM.CONFIG.UNUSEDPIN {Pullnone} [current_design]
- set_property CFGBVS GND [current_design]
- set_property CONFIG_VOLTAGE 1.8 [current_design]
- set_property BITSTREAM.CONFIG.OVERTEMPSHUTDOWN Enable [current_design]

Generate an MCS file with these properties (write_cfgmem):

- -format MCS
- -size 64
- -interface SPIx8
- -loadbit "up 0x0000000 <directory/to/file/filename.bit>" (0th location)
- -loadbit "up 0x2000000 <directory/to/file/filename.bit>" (1st location, optional)

Program with vivado hardware manager with these settings (see xapp1233):

- SPI part: mt25qu256-spi-x1_x2_x4_x8
- State of non-config mem I/O pins: Pull-none
- Target the four files generated from the write_cfgmem tcl command.

3.9.2 Configuration via JTAG

A micro-USB AB Cable may be attached to the front panel or rear edge USB port. This permits the FPGA to be reconfigured using the Xilinx Vivado Hardware Manager via the integrated Digilent JTAG converter box. The device will be automatically recognized in Vivado Hardware Manager.

For more detailed instructions, please see “Using a Vivado Hardware Manager to Program an FPGA Device” section of Xilinx UG908: https://www.xilinx.com/support/documentation/sw_manuals/xilinx2014_1/ug908-vivado-programming-debugging.pdf

3.10 GPIO Connector

The GPIO option consists of a versatile shrouded connector from Molex with part number 0878331220 that give users with custom IO requirements four direct connect to FPGA signals.

Recommended mating plug: Molex 0875681273

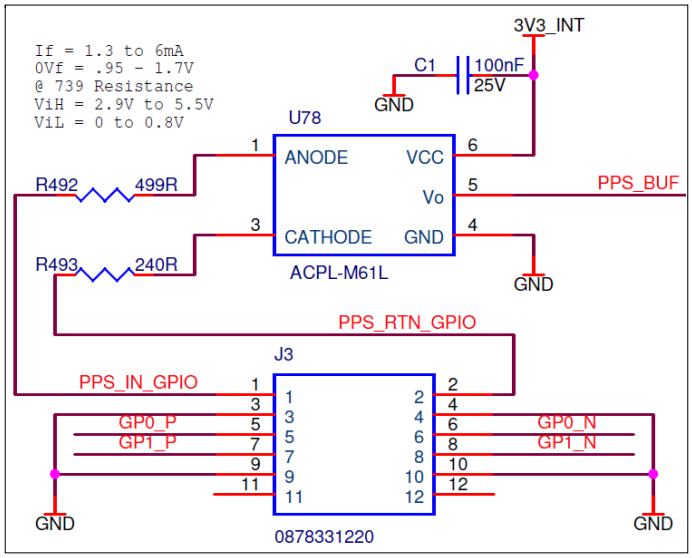

Figure 13 : GPIO Connector Schematic

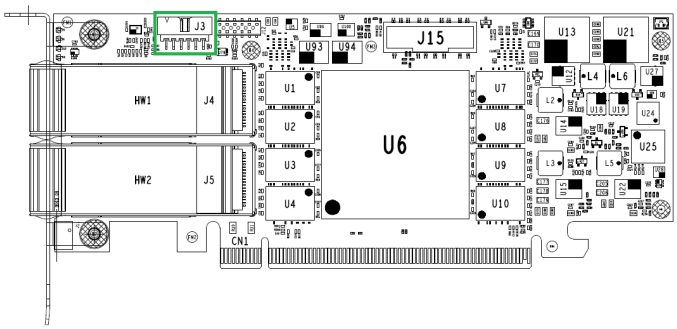

Figure 14 : GPIO Connector Location

3.10.1 Direct Connect FPGA Signals

Four nets are broken out to the GPIO header as two differential pairs. These signal are suitable for any 1.8V supported signaling standards supported by the Xilinx UltraScale architecture. See Xilinx UG571 for IO options. LVDS and 1.8 CMOS are popular options.

The direct connect GPIO signals are limited to 1.8V by a quickswitch (74CBTLVD3861BQ) in order to protect the FPGA from overvoltage on IO pins. This quickswitch allows the signals to travel in either direction with only 4 ohms of series impedance and less than 1ns of propagation delay. The nets are directly connected to the FPGA after the quickswitch.

Direct connect signal names are labeled GP0_1V8_P/N and GP1_1V8_P/N to show polarity and grouping. The signal pin allocations can be found in Complete Pinout Table

3.10.2 Timing Input

The first two pins of the GPIO connector can be used as an isolated timing input signal. Applications can either directly connect to the GPIO connector, or Alpha Data can provide a cabled solution with an SMA or similar connector on the front panel. Contact sales@alpha-data.com for front panel connector options.

For pin locations, see signal name PPS_BUF_1V8 in Complete Pinout Table.

The signal is isolated through a optical isolator part number ACPL-M61L with a 739 ohm of series resistance.

3.11 User EEPROM

A 2Kb I2C user EEPROM is provided for storing MAC addresses or other user information. The EEPROM is part number M24C02-RMC6TG.

The address pins A2, A1, and A0 are all strapped to a logical '0'.

Write protect (WP), Serial Clock (SCL), and Serial Data (SDA) pin assignments can be found in Complete Pinout Table with the names SPARE_WP, SPARE_SCL, and SPARE_SDA respectively.

WP, SDA, and SCL signals all have external pull-up resistors on the card.

Appendix A: Complete Pinout Table

Pin Number	Signal Name	Bank Voltage
AU24	AVR_B2U_1V8	1.8
AW26	AVR_HS_B2U_1V8	1.8
AV26	AVR_HS_CLK_1V8	1.8
AV24	AVR_HS_U2B_1V8	1.8
AV25	AVR_MON_CLK_1V8	1.8
AU25	AVR_U2B_1V8	1.8
AC34	CAPI_CLK_C_PIN_N	MGT_REFCLK
AC33	CAPI_CLK_C_PIN_P	MGT_REFCLK
AG34	CAPI_CLK_D_PIN_N	MGT_REFCLK
AG33	CAPI_CLK_D_PIN_P	MGT_REFCLK
D28	CAPI_I2C_SCL_1V8	1.8
C28	CAPI_I2C_SDA_1V8	1.8
AV37	CAPI_RX0_N	MGT
AV36	CAPI_RX0_P	MGT
AU39	CAPI_RX1_N	MGT
AU38	CAPI_RX1_P	MGT
AE39	CAPI_RX10_N	MGT
AE38	CAPI_RX10_P	MGT
AR39	CAPI_RX2_N	MGT
AR38	CAPI_RX2_P	MGT
AN39	CAPI_RX3_N	MGT
AN38	CAPI_RX3_P	MGT
AL39	CAPI_RX7_N	MGT
AL38	CAPI_RX7_P	MGT
AJ39	CAPI_RX8_N	MGT
AJ38	CAPI_RX8_P	MGT
AG39	CAPI_RX9_N	MGT
AG38	CAPI_RX9_P	MGT
AW34	CAPI_TX0_N	MGT
AW33	CAPI_TX0_P	MGT
AU34	CAPI_TX1_N	MGT
AU33	CAPI_TX1_P	MGT
AF36	CAPI_TX10_N	MGT

Table 16 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Bank Voltage
AF35	CAPI_TX10_P	MGT
AT36	CAPI_TX2_N	MGT
AT35	CAPI_TX2_P	MGT
AP36	CAPI_TX3_N	MGT
AP35	CAPI_TX3_P	MGT
AM36	CAPI_TX7_N	MGT
AM35	CAPI_TX7_P	MGT
AK36	CAPI_TX8_N	MGT
AK35	CAPI_TX8_P	MGT
AH36	CAPI_TX9_N	MGT
AH35	CAPI_TX9_P	MGT
AB10	CCLK	1.8
F9	DDR4_0_A0	1.2
G9	DDR4_0_A1	1.2
D9	DDR4_0_A10	1.2
H11	DDR4_0_A11	1.2
E8	DDR4_0_A12	1.2
J11	DDR4_0_A13	1.2
C9	DDR4_0_A14	1.2
B11	DDR4_0_A15	1.2
K12	DDR4_0_A16	1.2
H9	DDR4_0_A17	1.2
G11	DDR4_0_A2	1.2
D11	DDR4_0_A3	1.2
E12	DDR4_0_A4	1.2
G10	DDR4_0_A5	1.2
F10	DDR4_0_A6	1.2
J9	DDR4_0_A7	1.2
J8	DDR4_0_A8	1.2
F12	DDR4_0_A9	1.2
C12	DDR4_0_ACT_N	1.2
H7	DDR4_0_ALERT_N	1.2
F8	DDR4_0_BA0	1.2
H8	DDR4_0_BA1	1.2
D10	DDR4_0_BG0	1.2
E11	DDR4_0_BG1	1.2

Table 16 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Bank Voltage
B10	DDR4_0_C0	1.2
C11	DDR4_0_C1	1.2
A9	DDR4_0_C2	1.2
G12	DDR4_0_CK_C	1.2
H12	DDR4_0_CK_T	1.2
B9	DDR4_0_CKE	1.2
E10	DDR4_0_CS_N	1.2
N12	DDR4_0_DM0	1.2
P14	DDR4_0_DM1	1.2
G15	DDR4_0_DM2	1.2
D14	DDR4_0_DM3	1.2
E20	DDR4_0_DM4	1.2
B20	DDR4_0_DM5	1.2
H22	DDR4_0_DM6	1.2
N22	DDR4_0_DM7	1.2
J13	DDR4_0_DM8	1.2
L10	DDR4_0_DQ0	1.2
L9	DDR4_0_DQ1	1.2
M15	DDR4_0_DQ10	1.2
M17	DDR4_0_DQ11	1.2
M14	DDR4_0_DQ12	1.2
N18	DDR4_0_DQ13	1.2
N16	DDR4_0_DQ14	1.2
N17	DDR4_0_DQ15	1.2
F15	DDR4_0_DQ16	1.2
E16	DDR4_0_DQ17	1.2
F14	DDR4_0_DQ18	1.2
E17	DDR4_0_DQ19	1.2
N9	DDR4_0_DQ2	1.2
G16	DDR4_0_DQ20	1.2
F17	DDR4_0_DQ21	1.2
E15	DDR4_0_DQ22	1.2
G17	DDR4_0_DQ23	1.2
A17	DDR4_0_DQ24	1.2
C16	DDR4_0_DQ25	1.2
B16	DDR4_0_DQ26	1.2

Table 16 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Bank Voltage
A14	DDR4_0_DQ27	1.2
B17	DDR4_0_DQ28	1.2
B14	DDR4_0_DQ29	1.2
M9	DDR4_0_DQ3	1.2
D16	DDR4_0_DQ30	1.2
D15	DDR4_0_DQ31	1.2
F18	DDR4_0_DQ32	1.2
F20	DDR4_0_DQ33	1.2
F19	DDR4_0_DQ34	1.2
D21	DDR4_0_DQ35	1.2
E18	DDR4_0_DQ36	1.2
G19	DDR4_0_DQ37	1.2
E21	DDR4_0_DQ38	1.2
G20	DDR4_0_DQ39	1.2
M10	DDR4_0_DQ4	1.2
D18	DDR4_0_DQ40	1.2
B22	DDR4_0_DQ41	1.2
A19	DDR4_0_DQ42	1.2
A18	DDR4_0_DQ43	1.2
C19	DDR4_0_DQ44	1.2
B19	DDR4_0_DQ45	1.2
A22	DDR4_0_DQ46	1.2
C18	DDR4_0_DQ47	1.2
G22	DDR4_0_DQ48	1.2
J20	DDR4_0_DQ49	1.2
K11	DDR4_0_DQ5	1.2
H19	DDR4_0_DQ50	1.2
J19	DDR4_0_DQ51	1.2
H18	DDR4_0_DQ52	1.2
J18	DDR4_0_DQ53	1.2
G21	DDR4_0_DQ54	1.2
K18	DDR4_0_DQ55	1.2
L20	DDR4_0_DQ56	1.2
L18	DDR4_0_DQ57	1.2
N19	DDR4_0_DQ58	1.2
M21	DDR4_0_DQ59	1.2

Table 16 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Bank Voltage
M11	DDR4_0_DQ6	1.2
M19	DDR4_0_DQ60	1.2
M22	DDR4_0_DQ61	1.2
L19	DDR4_0_DQ62	1.2
M20	DDR4_0_DQ63	1.2
H16	DDR4_0_DQ64	1.2
K15	DDR4_0_DQ65	1.2
J16	DDR4_0_DQ66	1.2
J14	DDR4_0_DQ67	1.2
K13	DDR4_0_DQ68	1.2
L13	DDR4_0_DQ69	1.2
K10	DDR4_0_DQ7	1.2
H14	DDR4_0_DQ70	1.2
J15	DDR4_0_DQ71	1.2
L17	DDR4_0_DQ8	1.2
M16	DDR4_0_DQ9	1.2
L12	DDR4_0_DQS0_C	1.2
M12	DDR4_0_DQS0_T	1.2
L14	DDR4_0_DQS1_C	1.2
L15	DDR4_0_DQS1_T	1.2
E13	DDR4_0_DQS2_C	1.2
F13	DDR4_0_DQS2_T	1.2
A15	DDR4_0_DQS3_C	1.2
B15	DDR4_0_DQS3_T	1.2
E22	DDR4_0_DQS4_C	1.2
F22	DDR4_0_DQS4_T	1.2
B21	DDR4_0_DQS5_C	1.2
C21	DDR4_0_DQS5_T	1.2
K20	DDR4_0_DQS6_C	1.2
K21	DDR4_0_DQS6_T	1.2
K22	DDR4_0_DQS7_C	1.2
L22	DDR4_0_DQS7_T	1.2
K16	DDR4_0_DQS8_C	1.2
K17	DDR4_0_DQS8_T	1.2
A10	DDR4_0_ODT	1.2
G7	DDR4_0_PAR	1.2

Table 16 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Bank Voltage
F7	DDR4_0_RESET_N	1.2
J10	DDR4_0_TEN	1.2
AN9	DDR4_1_A0	1.2
AM9	DDR4_1_A1	1.2
AR8	DDR4_1_A10	1.2
AL10	DDR4_1_A11	1.2
AP8	DDR4_1_A12	1.2
AK11	DDR4_1_A13	1.2
AP9	DDR4_1_A14	1.2
AV10	DDR4_1_A15	1.2
AT11	DDR4_1_A16	1.2
AL8	DDR4_1_A17	1.2
AP11	DDR4_1_A2	1.2
AU9	DDR4_1_A3	1.2
AT10	DDR4_1_A4	1.2
AL12	DDR4_1_A5	1.2
AM12	DDR4_1_A6	1.2
AM10	DDR4_1_A7	1.2
AL11	DDR4_1_A8	1.2
AP7	DDR4_1_A9	1.2
AV9	DDR4_1_ACT_N	1.2
AR10	DDR4_1_ALERT_N	1.2
AN11	DDR4_1_BA0	1.2
AR9	DDR4_1_BA1	1.2
AP12	DDR4_1_BG0	1.2
AN10	DDR4_1_BG1	1.2
AW13	DDR4_1_C0	1.2
AU10	DDR4_1_C1	1.2
AW11	DDR4_1_C2	1.2
AN7	DDR4_1_CK_C	1.2
AM7	DDR4_1_CK_T	1.2
AU12	DDR4_1_CKE	1.2
AT12	DDR4_1_CS_N	1.2
AG12	DDR4_1_DM0	1.2
AK15	DDR4_1_DM1	1.2
AP16	DDR4_1_DM2	1.2

Table 16 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Bank Voltage
AV16	DDR4_1_DM3	1.2
AP21	DDR4_1_DM4	1.2
AU20	DDR4_1_DM5	1.2
AG19	DDR4_1_DM6	1.2
AL18	DDR4_1_DM7	1.2
AG14	DDR4_1_DM8	1.2
AK9	DDR4_1_DQ0	1.2
AK10	DDR4_1_DQ1	1.2
AL13	DDR4_1_DQ10	1.2
AM14	DDR4_1_DQ11	1.2
AL15	DDR4_1_DQ12	1.2
AM17	DDR4_1_DQ13	1.2
AL17	DDR4_1_DQ14	1.2
AM13	DDR4_1_DQ15	1.2
AR15	DDR4_1_DQ16	1.2
AP14	DDR4_1_DQ17	1.2
AT15	DDR4_1_DQ18	1.2
AR14	DDR4_1_DQ19	1.2
AH10	DDR4_1_DQ2	1.2
AP17	DDR4_1_DQ20	1.2
AN16	DDR4_1_DQ21	1.2
AN17	DDR4_1_DQ22	1.2
AN15	DDR4_1_DQ23	1.2
AU15	DDR4_1_DQ24	1.2
AT17	DDR4_1_DQ25	1.2
AV15	DDR4_1_DQ26	1.2
AT16	DDR4_1_DQ27	1.2
AV14	DDR4_1_DQ28	1.2
AW17	DDR4_1_DQ29	1.2
AJ11	DDR4_1_DQ3	1.2
AW14	DDR4_1_DQ30	1.2
AW18	DDR4_1_DQ31	1.2
AP19	DDR4_1_DQ32	1.2
AT20	DDR4_1_DQ33	1.2
AN21	DDR4_1_DQ34	1.2
AR19	DDR4_1_DQ35	1.2

Table 16 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Bank Voltage
AN20	DDR4_1_DQ36	1.2
AR18	DDR4_1_DQ37	1.2
AR20	DDR4_1_DQ38	1.2
AP18	DDR4_1_DQ39	1.2
AJ9	DDR4_1_DQ4	1.2
AW19	DDR4_1_DQ40	1.2
AU22	DDR4_1_DQ41	1.2
AV19	DDR4_1_DQ42	1.2
AW22	DDR4_1_DQ43	1.2
AU18	DDR4_1_DQ44	1.2
AT22	DDR4_1_DQ45	1.2
AW21	DDR4_1_DQ46	1.2
AU19	DDR4_1_DQ47	1.2
AH19	DDR4_1_DQ48	1.2
AJ22	DDR4_1_DQ49	1.2
AH12	DDR4_1_DQ5	1.2
AF21	DDR4_1_DQ50	1.2
AH22	DDR4_1_DQ51	1.2
AF20	DDR4_1_DQ52	1.2
AJ19	DDR4_1_DQ53	1.2
AH21	DDR4_1_DQ54	1.2
AJ21	DDR4_1_DQ55	1.2
AM19	DDR4_1_DQ56	1.2
AK20	DDR4_1_DQ57	1.2
AM22	DDR4_1_DQ58	1.2
AL22	DDR4_1_DQ59	1.2
AG10	DDR4_1_DQ6	1.2
AM20	DDR4_1_DQ60	1.2
AK19	DDR4_1_DQ61	1.2
AN19	DDR4_1_DQ62	1.2
AL20	DDR4_1_DQ63	1.2
AF15	DDR4_1_DQ64	1.2
AJ17	DDR4_1_DQ65	1.2
AH17	DDR4_1_DQ66	1.2
AJ14	DDR4_1_DQ67	1.2
AG15	DDR4_1_DQ68	1.2

Table 16 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Bank Voltage
AJ13	DDR4_1_DQ69	1.2
AJ12	DDR4_1_DQ7	1.2
AG17	DDR4_1_DQ70	1.2
AJ16	DDR4_1_DQ71	1.2
AM15	DDR4_1_DQ8	1.2
AN14	DDR4_1_DQ9	1.2
AH9	DDR4_1_DQS0_C	1.2
AG9	DDR4_1_DQS0_T	1.2
AL16	DDR4_1_DQS1_C	1.2
AK16	DDR4_1_DQS1_T	1.2
AT13	DDR4_1_DQS2_C	1.2
AR13	DDR4_1_DQS2_T	1.2
AV17	DDR4_1_DQS3_C	1.2
AU17	DDR4_1_DQS3_T	1.2
AP22	DDR4_1_DQS4_C	1.2
AN22	DDR4_1_DQS4_T	1.2
AV21	DDR4_1_DQS5_C	1.2
AV22	DDR4_1_DQS5_T	1.2
AH20	DDR4_1_DQS6_C	1.2
AG20	DDR4_1_DQS6_T	1.2
AL21	DDR4_1_DQS7_C	1.2
AK21	DDR4_1_DQS7_T	1.2
AH15	DDR4_1_DQS8_C	1.2
AH16	DDR4_1_DQS8_T	1.2
AR11	DDR4_1_ODT	1.2
AM8	DDR4_1_PAR	1.2
AN12	DDR4_1_RESET_N	1.2
AV11	DDR4_1_TEN	1.2
U9	DONE_1V8	1.8
AB15	DXN	1.8
AB16	DXP	1.8
AJ28	EMCCLK_B	1.8
AP27	FABRIC_CLK_PIN_N	1.8(DIFFTERM required)
AP26	FABRIC_CLK_PIN_P	1.8(DIFFTERM required)
AR26	FPGA_CPLD_SPARE	1.8
AE8	FPGA_FLASH_CE1_L	1.8

Table 16 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Bank Voltage
AV30	FPGA_FLASH_CE2_L	1.8
AB8	FPGA_FLASH_DQ0	1.8
AD8	FPGA_FLASH_DQ1	1.8
Y8	FPGA_FLASH_DQ2	1.8
AC8	FPGA_FLASH_DQ3	1.8
AF30	FPGA_FLASH_DQ4	1.8
AG30	FPGA_FLASH_DQ5	1.8
AF28	FPGA_FLASH_DQ6	1.8
AG28	FPGA_FLASH_DQ7	1.8
AH24	FRONT_LED_0	1.8
AJ23	FRONT_LED_1	1.8
F30	GP0_1V8_N	1.8
G30	GP0_1V8_P	1.8
H31	GP1_1V8_N	1.8
J31	GP1_1V8_P	1.8
N34	GTY_CLK_0B_PIN_N	MGT_REFCLK
N33	GTY_CLK_0B_PIN_P	MGT_REFCLK
U34	GTY_CLK_0C_PIN_N	MGT_REFCLK
U33	GTY_CLK_0C_PIN_P	MGT_REFCLK
AE34	GTY_CLK_1B_PIN_N	MGT_REFCLK
AE33	GTY_CLK_1B_PIN_P	MGT_REFCLK
AJ34	GTY_CLK_1C_PIN_N	MGT_REFCLK
AJ33	GTY_CLK_1C_PIN_P	MGT_REFCLK
T10	INIT_B_1V8	1.8
A30	INT_1V8	1.8
G32	MEM_CLK_0_N	1.8(Requires DIFFTERM)
G31	MEM_CLK_0_P	1.8(Requires DIFFTERM)
AN26	MEM_CLK_1_PIN_N	1.8(Requires DIFFTERM)
AN25	MEM_CLK_1_PIN_P	1.8(Requires DIFFTERM)
C29	OPTICAL_INT_1V8_L	1.8
B29	OPTICAL_RESET_1V8_L	1.8
A28	OPTICAL_SCL_1V8	1.8
A29	OPTICAL_SDA_1V8	1.8
AA6	PCIE_REFCLK_1_PIN_N	MGT_REFCLK
AA7	PCIE_REFCLK_1_PIN_P	MGT_REFCLK
AJ6	PCIE_REFCLK_2_PIN_N	MGT_REFCLK

Table 16 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Bank Voltage
AJ7	PCIE_REFCLK_2_PIN_P	MGT_REFCLK
J1	PCIE_RX0_N	MGT
J2	PCIE_RX0_P	MGT
L1	PCIE_RX1_N	MGT
L2	PCIE_RX1_P	MGT
AJ1	PCIE_RX10_N	MGT
AJ2	PCIE_RX10_P	MGT
AL1	PCIE_RX11_N	MGT
AL2	PCIE_RX11_P	MGT
AN1	PCIE_RX12_N	MGT
AN2	PCIE_RX12_P	MGT
AR1	PCIE_RX13_N	MGT
AR2	PCIE_RX13_P	MGT
AU1	PCIE_RX14_N	MGT
AU2	PCIE_RX14_P	MGT
AV3	PCIE_RX15_N	MGT
AV4	PCIE_RX15_P	MGT
N1	PCIE_RX2_N	MGT
N2	PCIE_RX2_P	MGT
R1	PCIE_RX3_N	MGT
R2	PCIE_RX3_P	MGT
U1	PCIE_RX4_N	MGT
U2	PCIE_RX4_P	MGT
W1	PCIE_RX5_N	MGT
W2	PCIE_RX5_P	MGT
AA1	PCIE_RX6_N	MGT
AA2	PCIE_RX6_P	MGT
AC1	PCIE_RX7_N	MGT
AC2	PCIE_RX7_P	MGT
AE1	PCIE_RX8_N	MGT
AE2	PCIE_RX8_P	MGT
AG1	PCIE_RX9_N	MGT
AG2	PCIE_RX9_P	MGT
H4	PCIE_TX0_PIN_N	MGT
H5	PCIE_TX0_PIN_P	MGT
K4	PCIE_TX1_PIN_N	MGT

Table 16 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Bank Voltage
K5	PCIE_TX1_PIN_P	MGT
AK4	PCIE_TX10_PIN_N	MGT
AK5	PCIE_TX10_PIN_P	MGT
AM4	PCIE_TX11_PIN_N	MGT
AM5	PCIE_TX11_PIN_P	MGT
AP4	PCIE_TX12_PIN_N	MGT
AP5	PCIE_TX12_PIN_P	MGT
AT4	PCIE_TX13_PIN_N	MGT
AT5	PCIE_TX13_PIN_P	MGT
AU6	PCIE_TX14_PIN_N	MGT
AU7	PCIE_TX14_PIN_P	MGT
AW6	PCIE_TX15_PIN_N	MGT
AW7	PCIE_TX15_PIN_P	MGT
M4	PCIE_TX2_PIN_N	MGT
M5	PCIE_TX2_PIN_P	MGT
P4	PCIE_TX3_PIN_N	MGT
P5	PCIE_TX3_PIN_P	MGT
T4	PCIE_TX4_PIN_N	MGT
T5	PCIE_TX4_PIN_P	MGT
V4	PCIE_TX5_PIN_N	MGT
V5	PCIE_TX5_PIN_P	MGT
AB4	PCIE_TX6_PIN_N	MGT
AB5	PCIE_TX6_PIN_P	MGT
AD4	PCIE_TX7_PIN_N	MGT
AD5	PCIE_TX7_PIN_P	MGT
AF4	PCIE_TX8_PIN_N	MGT
AF5	PCIE_TX8_PIN_P	MGT
AH4	PCIE_TX9_PIN_N	MGT
AH5	PCIE_TX9_PIN_P	MGT
AJ31	PERST_1V8_0_L	1.8
AH29	PERST_1V8_1_L	1.8
J30	POWER9_SCL_1V8	1.8
K30	POWER9_SDA_1V8	1.8
P30	PPS_BUF_1V8	1.8
B30	PRE_DETECT_1V8	1.8
V10	PROGRAM_B_1V8	1.8

Table 16 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Bank Voltage
U8	PUDC_B	1.8
F29	QSFP0_MODPRS_L	1.8
G39	QSFP0_RX0_N	MGT
G38	QSFP0_RX0_P	MGT
E39	QSFP0_RX1_N	MGT
E38	QSFP0_RX1_P	MGT
C39	QSFP0_RX2_N	MGT
C38	QSFP0_RX2_P	MGT
B37	QSFP0_RX3_N	MGT
B36	QSFP0_RX3_P	MGT
D31	QSFP0_SEL_1V8_L	1.8
F36	QSFP0_TX0_N	MGT
F35	QSFP0_TX0_P	MGT
D36	QSFP0_TX1_N	MGT
D35	QSFP0_TX1_P	MGT
C34	QSFP0_TX2_N	MGT
C33	QSFP0_TX2_P	MGT
A34	QSFP0_TX3_N	MGT
A33	QSFP0_TX3_P	MGT
F33	QSFP1_MODPRS_L	1.8
R39	QSFP1_RX0_N	MGT
R38	QSFP1_RX0_P	MGT
N39	QSFP1_RX1_N	MGT
N38	QSFP1_RX1_P	MGT
L39	QSFP1_RX2_N	MGT
L38	QSFP1_RX2_P	MGT
J39	QSFP1_RX3_N	MGT
J38	QSFP1_RX3_P	MGT
D30	QSFP1_SEL_1V8_L	1.8
P36	QSFP1_TX0_N	MGT
P35	QSFP1_TX0_P	MGT
M36	QSFP1_TX1_N	MGT
M35	QSFP1_TX1_P	MGT
K36	QSFP1_TX2_N	MGT
K35	QSFP1_TX2_P	MGT
H36	QSFP1_TX3_N	MGT

Table 16 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Bank Voltage
H35	QSFP1_TX3_P	MGT
R6	REFCLK100_PIN_N	MGT
R7	REFCLK100_PIN_P	MGT
L30	SI5328_1V8_SCL	1.8
L29	SI5328_1V8_SDA	1.8
M30	SI5328_REFCLK_IN_N	1.8 (LVDS)
M29	SI5328_REFCLK_IN_P	1.8(LVDS)
L34	SI5328_REFCLK_OUT0_PIN_N	MGT_REFCLK
L33	SI5328_REFCLK_OUT0_PIN_P	MGT_REFCLK
R34	SI5328_REFCLK_OUT1_PIN_N	MGT_REFCLK
R33	SI5328_REFCLK_OUT1_PIN_P	MGT_REFCLK
AT25	SPARE_SCL	1.8
AT26	SPARE_SDA	1.8
AP23	SPARE_WP	1.8
AW24	SRVC_MD_L_1V8	1.8
Y10	TCK	1.8
AC9	TDI	1.8
Y9	TDO	1.8
AD10	TMS	1.8
AT27	USER_LED_G0	1.8
AU27	USER_LED_G1	1.8
AU23	USER_LED_R	1.8
AV27	USR_SW0	1.8
AW27	USR_SW1	1.8

Table 16 : Complete Pinout Table

Revision History

Date	Revision	Changed By	Nature of Change
9 Sep 2016	1.0	K. Roth	Initial Release
6 Jan 2017	1.1	K. Roth	Added available power by rail table to Power Requirements, Added section: Custom Flash Write Interface, Updated clock termination recommendation to HSTL_I in Clocking, Added note about PCIe RX equalization options.
1 May 2017	2.0	K. Roth	Re-written to match rev3 PCB and support for OpenCAPI
21 Jun 2017	2.1	K. Roth	Updated all reference to DDR4 speeds at 16GB to be 2400MT/s and 32GB to be 1866MT/s.
14 Dec 2017	2.2	K. Roth	Removed inaccurate PERST location reference in PCI Express, Noted 312.5MHz limit in Clocking, removed reference to -2i speed grade,QSFP LP_MODE is now tied to GND, Moved section on timing input into GPIO section, removed references to u.fl connector, Modified LEDs with new front panel LEDs at rev6, Added clock AVR2UTIL examples in USB Interface, updated pinout appendix to include refclk100_pin and front_LED nets
3 Apr 2018	2.3	K. Roth	Added Si5328 diagram Si5328 Block Diagram, Added link to Xilinx documents for vivado hardware manager in Configuration via JTAG, updated Avr2util download link to point to current version.
15 May 2018	2.4	K. Roth	Updated Switch Functions to include SW2, Updated USB Interface description to mention rear USB connector (added in rev7 PCB).
6 Aug 2018	2.5	K. Roth	Product photo updated to rev8 PCB ,Updated Configuration From Flash Memory to remove inconsistent details about the fallback region location, reference to "tile 129" in QSFP28 corrected to "quad 127", all references to "mgt tile" changed to "mgt quad".
2 Oct 2018	2.6	K. Roth	Added Full Height Heat Sink
14 Dec 2018	2.7	K. Roth	Added Full Height Heat Sink
24 Oct 2019	2.8	K. Roth	Updated USB Interface to include linux FTP, Updated Configuration From Flash Memory to remove arbitrary flash address map.
24 Oct 2019	2.8	K. Roth	Updated USB Interface to include linux FTP, Updated Configuration From Flash Memory to remove arbitrary flash address map.

Date	Revision	Changed By	Nature of Change
14 Jan 2022	2.9	K. Roth	Removed references to I temperature grade and replaced them with E (which is standard), updated URL for avr2util download.
17 Jul 2023	2.10	K. Roth	Added Mechanical Dimensions (PCB only)

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